Web Results 1 - 10 of about 80,400 for simulation memory register verification instruction execution order dependencies conflicts. (0.40 seconds)

1. Microprocessors and Microsystems : An effective out-of-order ...

Some of examples of coprocessor **instruction execution** are given in Section 4. .... out-of-**order execution** with data **dependency** checking, resource **conflict** ...
linkinghub.elsevier.com/retrieve/pii/S0141933103000231 - Similar pages
by CH Jeong - 2003 - Cited by 1 - Related articles - All 8 versions

2. An SPU Reference Model for **Simulation**, Random Test Generation and ...

instruction simulator includes. **Memory**/**Register** dump. Breakpoint setting. Running program. Step **execution**. Show statistics such as number of **instructions** ...
ieeexplore.ieee.org/iel5/10626/33561/01594794.pdf - Similar pages

3. In-**order** issue out-of-**order execution** floating-point coprocessor ...

data **dependency** or resource **conflict** is found. Issued. **instructions** .... To implement this out-of-**order execution** control, the. **register** lock bits, pipeline ...
ieeexplore.ieee.org/iel5/7407/20118/00930119.pdf?arnumber=930119 - Similar pages
by K Seoul - 2001 - Cited by 4 - Related articles
More results from ieeexplore.ieee.org »

4. Microprocessor **Verification** Using Efficient Decision Procedures ...

an update to a **register** or **memory** location by one **instruction** may not be detected by an .... must be stalled due to resource **conflicts** or data **dependencies**. ...
www.springerlink.com/index/K3L52W598JU6704E.pdf - Similar pages
by RE Bryant - Cited by 4 - Related articles - All 7 versions

5. [PDF] Microprocessor **Verification** Using Efficient Decision Procedures ...

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of-**order execution**, **register** renaming, and many forms of caching [HP96]. **.... instructions** must be stalled due to resource **conflicts** or data **dependencies**. **...**

www.cs.cmu.edu/~bryant/pubdir/tableaux99.pdf - Similar pages

by RE Bryant - Cited by 4 - Related articles - All 7 versions

6. Parallel **execution** on the function-partitioned processor with **...**

The arc represents the **dependency** concern-. ing the **order** of **execution .... instruction** between **register** and **memory**, and. (3) is the **instruction** for the **...**

doi.wiley.com/10.1002/scj.4690220403 - Similar pages

7. **Simulation**/evaluation environment for a VLIW processor architecture

Aggressive in-**order** wide-issue **execution** leads to very long **instruction** word (VLIW) **....** dealing with issues such as **register dependencies** and operation **...**

www.research.ibm.com/journal/rd/413/moreno.html - 93k - Cached - Similar pages

by JH Moreno - 1997 - Cited by 21 - Related articles - All 6 versions

8. [PDF] Architectural Specification, Exploration and **Simulation** Through **...**

File Format: PDF/Adobe Acrobat - View as HTML

and only the Load and Store **instructions** can access **memory**, with respect to a base processor. (single-cycle, non-pipelined, in-**order execution** model) [13]. **...**

www.unab.edu.co/editorialunab/revistas/rcc/pdfs/r32_art2_c.pdf - Similar pages

by M Ayala-Rincon - Cited by 6 - Related articles - All 10 versions

9. A Practical Methodology for the Formal **Verification** of RISC Processors

In **order** to show that the sequential **execution** of each **instruction** is correctly **.....** cessor or to the contents of the data **memory**. Such data **dependencies ...**

www.ingentaconnect.com/content/klu/form/1998/00000013/00000002/00180577?crawler=true - Similar pages

by V GmbH - 1998 - Related articles

10. Developing the AMD-K5 Architecture

True operand **dependencies**, rather than program **instruction order**, largely determine **....** The major blocks in the **execution** core are the **register** file, **...**

doi.ieeecomputersociety.org/10.1109/40.491459 - Similar pages

1 2 3 4 5 6 7 8 9 10 Next

Results **1** - **10** of about **967** for **simulation** "**reference model**" **compare memory file dump register**. (**0.12** seconds)

1. An SPU **Reference Model** for **Simulation**, Random Test Generation and ...

The **simulator** gets commands via. command prompt or command **files**. Commands for the. instruction **simulator** includes. **Memory**/**Register dump**. Breakpoint setting **...**
ieeexplore.ieee.org/iel5/10626/33561/01594794.pdf - Similar pages

2. I'm Done Simulating; Now What? Verification Coverage Analysis and ...

Reference Model Comparison. **Register File** Trace **Compare**. 8%. **Memory** State **Compare ....** Fault **simulation** was not used for functional verification of the **...**
ieeexplore.ieee.org/iel3/3826/11178/00545595.pdf?arnumber=545595 - Similar pages
by M Kantrowitz - 1996 - Cited by 94 - Related articles - All 5 versions
More results from ieeexplore.ieee.org »

3. Postsilicon Validation Methodology for Microprocessors

Presilicon validation effort has predominantly used **simulation**, **....** Both references generate **compare files** of the end-of-test **memory** image in a compatible **...**
doi.ieeecomputersociety.org/10.1109/54.895008 - Similar pages
by H Rotithor - 2000 - Related articles

4. [PDF] AVM Based Unified Verification Platform In SystemC

File Format: PDF/Adobe Acrobat - View as HTML
I/O. Other scripts were used to **compare** the **simulation** result against a golden **....** this function can load content of a **file** to the **memory**. SAVE_MEM, **...**
www.mentorg.com.cn/eletter/0701/pdf/AVM.pdf - Similar pages

5. [PDF] Feldstein SPARC-V9 **Simulator** Version 1.0 Software Requirements ...

File Format: PDF/Adobe Acrobat - View as HTML
1.9.6.1 Change contents of any **memory** address prior to **simulation** run **...** Makes it possible to **dump** binary traces of internal signal activity to a **file** for **...**
www.alanfeldstein.com/products/software/iss/Feldstein_SPARC-V9_**Simulator**_SRS.pdf - Similar pages

6. Accelerating system integration by enhancing hardware, firmware ...

At this time, a **dump** of all latch values is written to a **file** and used in all **...** the corresponding engine, **register** #1 is updated in the **reference model**, **...**
www.research.ibm.com/journal/rd/483/schubert.html - 70k - Cached - Similar pages
by KD Schubert - 2004 - Cited by 5 - Related articles - All 5 versions

7. [PDF] Accelerated Verification of Digital Devices Using VHDL

File Format: PDF/Adobe Acrobat
simulation was stored as a reference **file**, and **files** resulting **.....** instructions between **register dumps**, errors might be masked **...**
ftp://ftp.estec.esa.nl/pub/vhdl/doc/AccVHDL.pdf - Similar pages

by S Habinc - Cited by 2 - Related articles - All 2 versions

8. Chapter 16 SYMBOLIC MODEL CHECKING AND **SIMULATION** WITH TEMPORAL ...

coverage or towards smaller **memory** footprint and faster runtime. **....** behavior r . SystemC **simulation**. AG(c r). Trigger states. **dump file ...**
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9. Copyright 2007, by the Association for Computing Machinery, Inc ...

... languages Optimization **Simulation** Verification B.5.3 Reliability and **....** Segmentation** Storage hierarchies Swapping** Virtual **memory** D.4.3 **File ...**
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10. THE ACM COMPUTING CLASSIFICATION SYSTEM Copyright 1995 by ...

... Data communications Open System Interconnection **reference model** (OSI) **...** hierarchies Swapping Virtual **memory** D.4.3 **File** Systems Management (E.5) Access **...**
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1. A simulation-based approach to architectural **verification** of **...**

the **design** of the **processor** units. On the other hand. architectural **verification** allows. **verification** to be performed at the program level by observing **...**
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2. Functional **design verification** for the PowerPC 601 microprocessor **...**

PPC601. were built. directly from. the. **processor**. **design**,. memory and **.....** and **memory coherency** monitors were designed and **...**
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3. Hot Chips 2008: **Memory Coherency** Over Networks—Can that Possibly **...**

Any **processor** can restart any stalled task because of the coherent memory. **...** Alas, my aged mental facilities and decrepit system-**design** skills are showing **...**
www.edn.com/blog/980000298/post/450032245.html - Similar pages

4. Functional **Verification** of a Multiple-issue, Out-of-Order **...**

exercising the **processor** to its **design** limits and thereby. exposing bugs that would not be readily detected using. simulation-based **verification** techniques. **...**
doi.ieeecomputersociety.org/10.1109/DAC.1998.10065 - Similar pages
by S Taylor - Cited by 54 - Related articles - All 14 versions

5. EETimes.com - New simulation capabilities advance SystemVerilog

May 16, 2005 **...** Another breakthrough, Agarwala said, is **memory coherency**. This avoids "collisions" in which multiple **design** blocks simultaneously write to **...**
www.eetimes.com/news/**design**/showArticle.jhtml?articleID=163101471 - 59k - Cached - Similar pages

6. Just like being there: Papers from the Fall **Processor** Forum 2005 **...**

Dec 6, 2005 **...** This Fall **Processor** Forum paper explores the customized IBM PowerPC **...** and **verification** process throughout the **design** of the system. **...**
www-128.ibm.com/developerworks/power/library/pa-fpfxbox/ - 51k - Cached - Similar pages

7. Method and system for **verifying** execution order within a **...**

An important aspect of both the **design** and testing of multiprocessor data processing systems is **verification** of correct implementation of a selected memory **...**
www.freepatentsonline.com/5692153.html - Similar pages
by N Malik - 1997 - Cited by 3 - Related articles - All 3 versions

8. **[PDF]** Product Engineer [Job ID# M102]

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Experience in **processor design** from a circuit level **....** such as I/O interfaces, network protocols, **memory coherency**, bus. protocols and high speed serial **...**
www.nacsa.com/archives/files/2006_job_fair/PASemi.pdf - Similar pages

9. Technical Resume: Embedded Developer

Dec 10, 2007 **... verification** methodology. Maximized **processor** performance by writing **...** The testbenches covered **memory coherency**, address translation, **...**
www.devbistro.com/resumes/rgtgdgag - Similar pages

10. **[PDF]** DDR Memory Systems at the Heart of Consumer Electronics

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while maintaining relative priority and **memory coherency**. **...** greater investment in **design** and **verification**. As the number of features grow, adding a **...**
www.ocpip.org/pressroom/articles/Recently_Published_Articles/OCP-Denali-122006.pdf - Similar pages

1. LNCS 4144 - Fast and Generalized Polynomial Time **Memory** ...

Verifying processor execution against its stated **memory consistency** model is an im-. portant problem in both **design** and silicon system **verification**. **...**
www.springerlink.com/index/922p1q12637m6722.pdf - Similar pages
by A Roy - Cited by 1 - Related articles - All 4 versions

2. Sudheendra Hangal's home page

Sun's **Processor** Roadmap, TSOtool, DIDUCE, IODINE, **Verifying Memory Consistency**, Dynamic Analysis (coming soon). Pet Peeves and what's cool: **...**
xenon.stanford.edu/~hangal/ - 10k - Cached - Similar pages

3. Generating Concurrent Test-Programs with Collisions for Multi ...

Generating concurrent testprograms with collisions for multi-**processor verification**. In IEEE International High Level **Design** Validation and Test Workshop, **...**
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4. [PPT] Dynamic **Verification** of **Memory Consistency** in Cache Coherent ...

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Orthogonal to static **verification**. Detects **design** bugs, not operating errors. What invariant can be used for **verification**? **Memory Consistency ...**
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5. [PDF] Shared **memory consistency** protocol **verification** against weak ...

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protocol **processor**. In [22, 23], shared **memory consistency** models are described. in an operational style. In [6], sequential consistency **verification**, **...**
www.cs.utah.edu/formal_**verification**/papers/cav02paper.pdf - Similar pages
by P Chatterjee - Cited by 11 - Related articles - All 6 versions

6. On the Decidability of Shared **Memory Consistency Verification**

processor, also known as the program order. On the other **.....** Formal **design** and **verification**. methods for shared memory systems. PhD thesis, Uni- **...**
ieeexplore.ieee.org/iel5/9956/32009/01487915.pdf - Similar pages
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7. What is Itanium **Memory Consistency** from the Programmer's Point of **...**

A formal specification of the intel itanium **processor** family memory ordering. **...** Hardware **Design** and **Verification** Methods (CHARME03), pages 81--95, 2003 **...**
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8. **[PPT]** Dynamic **Verification** of Sequential Consistency

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Verifying memory consistency = **Verifying** correctness of the memory system **...** Trivially observed on in-order **processor** with coherent caches **...**
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9. **[PDF]** A General Framework for Dynamic **Verification** of **Memory Consistency ...**

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Dynamic **Verification** of **Memory Consistency** in Cache-Coherent **.....** Checker **Processor Design**. In Proc. of the 33rd Annual **...**
www.ee.duke.edu/~sorin/papers/dsn06_dvmc.pdf - Similar pages
by A Meixner - Cited by 8 - Related articles - All 7 versions

10. **[PPT]** Some Challenges in Parallel and Distributed Hardware **Design** and **...**

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Some Challenges in Shared Memory **Processor Design**. and SMP / Distributed Programming **...** Small configuration **verification** of Shared **Memory Consistency ...**
www.csl.sri.com/users/shankar/VGC05/ganesh.ppt - Similar pages

Results **1** - **10** of about **78** for **processor verification design "memory consistency" repetitive**. (**0.10** seconds)

1. First Silicon Functional Validation and Debug of Multicore ...

lisions for multi-**processor verification**," in Proc. IEEE Int. High Level. **Design** Validation Test Workshop, 2002, pp. 27–29. **...**
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2. Formal Automatic **Verification** of Cache Coherence in ...

In every step of a state-based **verification** model, any **processor** can issue a load or a **.....** and **verification**, with a focus on **memory consistency** models, **...**
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3. http://www.cs.columbia.edu/resources/video/2007/spring

Because of this **processor**/memory performance gap -- often called the memory **...** memory system **design** paradigm where hardware mechanisms observe **repetitive ...**
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4. UT-Austin Computer Architecture Seminar Schedule Abstracts

He recently published the book "Modern **Processor Design**: Fundamentals of Superscalar **....** can bridge the performance gap among **memory consistency** models. **...**
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5. Parallel Computing : Performance analysis of the simultaneous ...

Their performance depends on how restrictive the **memory consistency** model is. **.....** low **design verification** effort and allow boundary optimization. **...**
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based **verification** model, any **processor** can issue a load or a store unless it **....** enough to apply to other protocols under relaxed **memory consistency** mod- **...**
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however the cost of buffering and speculation **verification**. hardware can be prohibitively expensive. We present the **design** of a combined hardware/software **...**
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Issues in Branch performance, Synchronization in Multiprocessing, High Performance **Processor Design** Issues: Pipeline **design**, Memory system **design**, **...**
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4713755, Cache **memory consistency** control with explicit software **....** The **processor** specifies the pack number when it reads or writes a cache resident pack. **...**
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Multiprocessors should support simple **memory consistency** models. **.....** product groups to spend much more effort in **verification** than in **design**. **...**
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... that ROBDD-based **verification** methods often take too long, or run out of **memory**, when applied to ... In this case the CPU time needed for **verification** is of ...
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... must shift toward more hands-on, design-oriented **instruction**. ... Increasing the amount of **memory** is also available ... is a symbolic and numeric **processor** that also ...
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Methods, apparatus and computer program products for determining equivalencies between integrated ...
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... **memory** that can direct a **processor** or other ... the specified functions and program **instruction** means for ... control of the post-layout **verification** system can be ...
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... skills without the benefit of for- mal **instruction**. ... schedule before any wind-tunnel **verification** was undertaken. ... N h , for which the vector **processor** has the ...
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Key authors: F Corella - C Fletcher - J Bauer - A Bodge - S Huberman

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Key authors: **J Mcmullan** - **D Hoder** - **D Huntley** - **D Naddor** - **R Beyers**

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RAPTOR: a single chip multiprocessor
SW Lee, YS Song, SW Kim, HC Oh, WJ Hahn - ASICs, 1999. AP-ASIC'99. The First IEEE Asia Pacific ..., 1999 - ieeexplore.ieee.org
... This **simulation** environment allows the **verification** stimuli to **...** the pseudorandom test based **verification** method with **...** of implementing the **processor** with current **...**
Cited by 8 - Related articles - Web Search - All 3 versions

Speculative execution of test patterns in a random test generator
D Weir, RC Brockmann - US Patent 5,729,554, 1998 - freepatentsonline.com
... test generator 2 and can be used in the **verification** of a complex design such as a CPU. **...** the current behavioral model state to the pre-**simulation** state in **...**
Cited by 15 - Related articles - Web Search - All 3 versions

Verification of accesses in a functional model of a speculative out-of-order computer system

GS Averill - US Patent 5,815,688, 1998 - Google Patents

... BEHAVIORAL MODEL \J STATE ADVANCE **SIMULATOR** TO POINT **...** present invention relates generally to **verification** methods for **...** been developed to increase **processor** speeds **...**

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A study on logic design and architecture simulator design of a newon-chip multiprocessor

WJ Hahn, K Park, SH Choi, SH Yoon - TENCON 99. Proceedings of the IEEE Region 10 Conference, 1999 - ieeexplore.ieee.org

... including 16Kbytes on-chip cache for each general **processor**. **...** Figure 3. **Verification** Model As shown in Figure 3, we built the **simulation** model by adding **...**

Related articles - Web Search - All 2 versions

[BOOK] ATUM: a new technique for capturing address traces using microcode

A Agarwal, RL Sites, M Horowitz - 1986 - IEEE Computer Society Press Los Alamitos, CA, USA

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AE32000: an embedded microprocessor core

HC Oh, HG Kim, HS Jung, JW Lee, BJ Kim, JY Jung, ... - ASICs, 2000. AP-ASIC 2000. Proceedings of the Second IEEE ..., 2000 - ieeexplore.ieee.org

... as SPEC is used by workstation-**processor** vendors. **...** LM.Noack., " I'm Done **Simulation**; Now What **...** **Verification** Coverage Analysis and Correctness Checking of the **...**

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Key authors: **D Geist** - **A Agarwal** - **G Biran** - **T Arons** - **M Slavkin**

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1. Logical **verification** of the NVAX CPU chip design - Computer Design ...

model, a copy of **register file** contents to **memory**). At .... Finally, the **memory dump**. area **file** from the **simulation** was compared ...
ieeexplore.ieee.org/iel2/442/6840/00276276.pdf?arnumber=276276 - Similar pages

2. I'm Done Simulating; Now What? **Verification** Coverage Analysis and ...

Cache **Coherency** Checkers. 9%. Reference Model Comparison. **Register File** Trace Compare .... Fault **simulation** was not used for functional **verification** of the ...
ieeexplore.ieee.org/iel3/3826/11178/00545595.pdf?arnumber=545595 - Similar pages
by M Kantrowitz - 1996 - Cited by 94 - Related articles - All 5 versions
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3. **Verification** of the UltraSPARCTM Microprocessor

during a regression, the value change **dump file**, along. with **simulation** logs, would be ..... **memory** arrays (caches, **register files**, etc.> were imple- ...
doi.ieeecomputersociety.org/10.1109/CMPCON.1995.512422 - Similar pages
by S Mehta - 1995 - Cited by 13 - Related articles

4. [PDF] "ESP-CV not only gave us the capacity to verify large **memory** ...

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severe limitations on complete **verification** of a custom **memory** ... structures, **register files** and some custom datapath designs. Unlike. the **verification** ...
www.synopsys.com/products/esp/sun_ss.pdf - Similar pages

5. Whitepapers

Because they are unfamiliar with logic **simulation** and emulation tools, they pass **memory** image **files** to the **verification** engineers who run the test. ...
www.verisity.com/resources/whitepaper/hwswco**verification**.html - 60k - Cached - Similar pages

6. THE ACM COMPUTING CLASSIFICATION SYSTEM Copyright 1995 by ...

... models **Simulation Verification** Worst-case analysis B.4.5 Reliability, ... hierarchies Swapping Virtual **memory** D.4.3 **File** Systems Management (E.5) ...
projects.csail.mit.edu/jacm/CR/1991/cr91.txt - 30k - Cached - Similar pages

7. [PDF] Feldstein SPARC-V9 **Simulator** Version 1.0 Software Requirements ...

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verification may be performed at **simulation** time. Produces trace **files** of ... Run-time **coherency** monitor/protocol checker. 1.6.7.5.4.2 **Memory** and Cache ...
www.alanfeldstein.com/products/software/fss/Feldstein_SPARC-V9_**Simulator**_SRS.pdf - Similar pages

8. Copyright 2007, by the Association for Computing Machinery, Inc ...

(NEW) Protocol architecture (OSI model) (REVISED) Protocol **verification** Routing .... Segmentation** Storage hierarchies Swapping** Virtual **memory** D.4.3 **File ...**
www.acm.org/about/class/ccs98.txt - 48k - Cached - Similar pages

9. Computing-Reviews-Klassifikation

Performance Analysis and Design Aids **Simulation Verification** Worst-case ..... Intelligence **Coherence** and coordination Languages and structures I.2.m. **...**
www.informatik.uni-leipzig.de/websql.dir/biblio/CRKlassifikation.html - 44k - Cached - Similar pages

10. General Literature General Biographies and Autobiographies ...

Protocol Architecture (OSI model) Protocol **Verification** Routing Protocols **...** Storage Hierarchies Swapping Virtual **Memory File** Systems Management It is **...**
139.91.183.30:9090/RDF/VRP/Examples/ACM-CSS.rdf - 231k - Cached - Similar pages

1 2 3 4 5 6 7 8 9 10 **Next**

Results **1** - **10** of about **4,170** for **simulation memory register content dump verification consistency model**. (**0.09** seconds)

1. Automatic Generation of High Performance Embedded **Memory Models** ...

embedded **memory models** used in RTLs) is designed. for **simulation** speed, and functional accuracy. **.....** **verification** tools to double-check the **consistency** of **...**
ieeexplore.ieee.org/iel5/4022212/4022213/04022237.pdf?isnumber=4022213&prod=CNF&arnumber=4022237&arSt... - Similar pages
by J Bhadra - Related articles - All 3 versions

2. **Verification** Methodology Of Compatible Microprocessors - Design ...

... register values, micro-operations and. **memory content** on the screen. The designers eradicate **...** comparing the two **models**' **consistency** and obviated the **...**
ieeexplore.ieee.org/iel3/4762/13192/00600108.pdf?arnumber=600108 - Similar pages
by JS Yim - 1997 - Cited by 6 - Related articles
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3. [PDF] Design **Verification** Of Complex Microprocessors - Circuits and ...

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CMV for the **verification** of C **model**. Co-**simulation** Environment. Polaris **....** codes and **memory content** on the screen as shown. in Fig. 7. **...**
vswww.kaist.ac.kr/~kyung/html/Paper/International%20Journal/IJ-45.pdf - Similar pages
by J Yim - 1921 - Cited by 3 - Related articles - All 7 versions

4. [PDF] Design **Verification** Of Complex Microprocessors - Circuits and ...

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the **verification** of C **model**. C. Reference **Model**. Co-**simulation** Environment **.... register** values, inicro-. codes and **memory content** on the screen **...**
ics.kaist.ac.kr/ver3.0/intjpapers/Design%20**Verification**%20of%20Complex%20Microprocess... - Similar pages

5. Accelerating system integration by enhancing hardware, firmware ...

The majority of **verification** tests ran on these **models**. **....** The terms hardware/ firmware (HW/FW) co-**simulation** and VPO imply that this activity begins **...**
www.research.ibm.com/journal/rd/483/schubert.html - 70k - Cached - Similar pages
by KD Schubert - 2004 - Cited by 5 - Related articles - All 5 versions

6. Using Term Rewriting Systems to Design and Verify Processors

Thus, rf[r] refers to the **content** of **register** r, and rf[r := v] represents **.....** For example, elsewhere we have defined a new **memory model** and associated **...**
doi.ieeecomputersociety.org/10.1109/40.768501 - Similar pages
by XS Arvind - 1999 - Cited by 15 - Related articles

7. [PDF] A "Flight Data Recorder" for Enabling Full-system Multiprocessor ...

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default **memory model**, our **simulator** implements Sequen-. tial **Consistency** as a correct implement of TSO. We **model**. a MOSI

directory protocol, similar to that **...**
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8. **[PDF]** Term-Level **Verification** of a Pipelined CISC Microprocessor

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from HCL to C to construct **simulation models** of the two processors, **.....** (C) requires **register consistency** within each stage as well as that ret **...**
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by RE Bryant - Cited by 2 - Related articles - All 4 versions

9. Method and apparatus for creating a multiprocessor **verification ...**

The **simulation models** usually include one or more various subsystems, **.....** The system state may include the **register** contents, cache and **memory** contents **...**
www.freepatentsonline.com/5740353.html - Similar pages
by JT Kreulen - 1998 - Cited by 16 - Related articles - All 3 versions

10. Instruction-Set **Simulation** and Tracing

More modular hardware **simulator** interfaces that simplify the process of adding new processor, **memory** system, and device **models**. **...**
xsim.com/bib/index1.d/index.html.gz - 311k - Cached - Similar pages